AMENDMENTS TO THE CLAIMS

(The following includes a complete listing of all claims with their current status indicated. Additional language is underscored; deletions are stricken through.)

Claims 1-14 (Canceled)

15. (Currently Amended) A multiple gate transistor structure comprising:

~~a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate:~~

C1

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed over said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer wherein said first and second gates cooperate to operate a single transistor.

16. (Previously Presented) A multiple gate transistor as claimed in claim 15 wherein said spacer is formed on a first side of said gate structure to form a second gate and a second side of said gate structure to form a third gate, said second contact being to said conductive portion of said spacer defining said second gate and said multiple gate transistor further comprising a third contact to said conductive portion of said spacer defining said third gate.

17. (Currently Amended) A two gate transistor structure comprising:

~~a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;~~

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a first contact to said gate structure; and

a second contact to said conductive portion of said first portion of said spacer wherein said first and second gates cooperate to operate a single transistor.

18. (Currently Amended) A three gate transistor structure comprising:

~~a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;~~

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a second portion of said spacer formed on a second side of said gate structure on said secondary oxide layer, at least a portion of said second portion of said spacer adjacent to said secondary oxide layer being conductive and defining a third gate;

a first contact to said gate structure;

a second contact to said conductive portion of said first portion of said spacer; and

a third contact to said conductive portion of said second portion of said spacer wherein said first, second, and third gates cooperate to operate a single transistor.

19. (Currently Amended) An integrated circuit structure comprising:

a first plurality of conventional transistors; and

a second plurality of transistors each comprising:

~~a gate structure formed on a first oxide layer on a semiconductor structure;~~

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed on said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer wherein said first and second gates cooperate to operate a single transistor and[[,]] said first plurality of conventional transistors and said second plurality of transistors [[being]] are interconnected to form said integrated circuit structure.

Claims 20-22 (Canceled)

C1

23. (Currently Amended) A transistor structure comprising:

~~an actual gate and a pseudo gate formed on a first oxide layer on a semiconductor structure, said actual and pseudo gates being separated from one another;~~

a first oxide layer formed on said semiconductor substrate;

a gate structure formed on said first oxide layer defining a first actual gate and a first pseudo gate;

a secondary oxide layer formed over said actual and pseudo gates;

a spacer formed on at least one side of said actual gate and on said pseudo gate on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said actual gate; and

a second contact to said conductive portion of said spacer at said pseudo gate, wherein said first and second actual gates cooperate to operate a single transistor.

Claims 24-32 (Canceled)

33. (New) A transistor device having multiple gates comprising:

a first source/drain region formed in a semiconductor substrate;

a second source/drain region formed in said semiconductor substrate spaced from said first source/drain region;

a gate structure including a first oxide layer formed between said first and second

source/drain regions defining a first gate of a transistor;

a secondary oxide layer formed over at least a portion of said gate structure;

a spacer formed over at least a portion of said gate structure and said second oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate of said transistor;

C1

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer wherein said first and second gates cooperate to operate said single transistor by affecting said first and second source/drain regions.